REMARKS/ARGUMENTS

In the Office Action mailed February 19, 2009, claims 1-15 and 17-25 were rejected. In response, Applicant hereby requests reconsideration of the application in view of the proposed amendments and the below-provided remarks. No claims are added or canceled. Applicant submits that the proposed amendments place the present application in condition for allowance or in better condition for appeal.

For reference, proposed amendments are submitted for claims 1 and 17. In particular, the proposed amendments for claim 1 are presented to clarify that the first write data and first address information are stored to the register. The proposed amendments for claim 1 are also presented to recite the pending write request, which includes second address information and second write data, is stored in the register. The proposed amendments for claim 1 are also presented to clarify when the write operation forwards the first write data from the register to the memory. Similar proposed amendments are presented for claim 17. These proposed amendments are supported, for example, by the subject matter described in the specification at page 3, line 30, through page 4, line 14, of the present application.

Claim Rejections under 35 U.S.C. 112

Claims 1-15 and 17-25 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action states that it is not clear whether the first write data would ever be stored in the register.

Applicant submits that independent claims 1 and 17 are each amended to clarify the language of the claims, including clarification that the first write data and the first address information are stored to the register. Hence, the present language of the claims clearly indicates that the first write data is stored in the register. Therefore, Applicant respectfully submits that the language of claims 1 and 17 is definite because the language particularly points out and distinctly claims that the first write data is stored in the register. Accordingly, Applicant respectfully requests that the rejections of claims 1-15 and 17-25 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-5, 9-14, 17-20, 24, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Norman (U.S. Pat. No. 6,438,665, hereinafter Norman) in view of Magro (U.S. Pat. No. 6,151,658, hereinafter Magro). Additionally, claims 6-8 and 21-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Norman, in view of Magro, and further in view of Reams (U.S. Pat. No. 6,438,660, hereinafter Reams). Additionally, claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over Norman, in view of Magro, and further in view of Sunaga et al. (U.S. Pat. No. 6,785,154, hereinafter Sunaga). However, Applicant respectfully submits that these claims are patentable over Norman, Magro, Reams, and Sunaga for the reasons provided below.

Clarification of the Rejections

As a preliminary matter, Applicant appreciates the Examiner's clarification as to the reasoning used as the basis of the rejection of claim 1. In particular, the Examiner clarifies in the present Office Action that Magro is specifically relied on as teaching the operation of ascertaining whether the first address information is stored in said register.

In the previous Office Action, the Examiner seemed to refer to Norman as purportedly teaching determining if first and second write data are different, but did not appear to address comparing first write data with second write data in a register. Moreover, the Examiner stated generally that Magro taught a limitation related to the register, within the context of both 1) ascertaining whether the first address information is stored in the register and, if yes, 2) comparing the first write data with second write data of an earlier write request in the register. Office Action 10/03/08, page 10, lines 9-12. Similarly, the Examiner stated in the previous Office Action that Magro demonstrated both 1) ascertaining the first address information is in the register and 2) comparing the first write data with the second write data allocated to the first address. Office Action 10/03/08, page 14, lines 17-20. These same statements are found in the present Office Action mailed 2/19/09 at page 13, lines 7-10, and page 15, lines 13-16. Additionally, the present Office Action specifically asserts that Magro teaches comparing the first and second write data. Office Action 2/19/09, page 16, line 12, through page 17, line 3. From these references in the previous and present Office Actions, it appeared that the

Examiner was relying on Magro as purportedly teaching operations for both 1) ascertaining and 2) comparing, as recited in the claim.

Based on these many references to Magro as purportedly teaching comparing first and second write data, it seems excessive to state that Applicant's previous remarks might have been "completely off the mark," "irrelevant," or an "incorrect allegation." Applicant was merely trying to respond to the specific arguments regarding Magro presented by the Examiner in the previous Office Action.

Nevertheless, the Examiner clarifies in the present Office Action that the Examiner relies on Magro as merely teaching the operation of ascertaining whether first address information is stored in the register. Office Action 2/19/09, page 6, lines 20-22. The Examiner does not rely on Magro as teaching comparing whether first write data is different from second write data. Office Action 2/19/09, page 6, lines 16-19. Applicant expresses appreciation to the Examiner for this clarification, as it will allow Applicant to engage in more meaningful discussion with the Examiner regarding the specific reasoning asserted in support of the rejection.

Independent Claim 1

Claim 1 recites "ascertain whether said first address information is equal to second address information for a pending write request stored in said register, wherein said pending write request comprises said second address information and corresponding second write data" and "determine if said first write data stored in said register is different from said second write data of said pending write request stored in said register" (emphasis added).

For a proper understanding of this subject matter in the claim, it should be noted that the ascertaining operation is between first and second address information. In contrast, the comparison operation is between first and second write data. The write data is different from corresponding write addresses, or address information. The first write data is received as part of a write request. In contrast, the second write data is from a pending write request—prior to the write request which includes the first write data. The second write data is stored in the register, which is a temporary storage. Since there is a cost associated with writing data to memory, the register can be used to temporarily store

the second write data and the first write data before the first write data is possibly written to the memory or, alternatively, discarded. As explained in the specification of the present application, in certain embodiments the first write data is written from the register to the memory only if the first write data is different from data already stored in the memory at the address corresponding to the first write address information. Page 4, lines 9-14. While the details of the specification are not read into the claims, this general overview of the subject matter described in the specification should be useful to provide a contextual example of the terminology and language in the claim.

Applicant submits that claim 1 of the present application is patentable over the combination of cited references because the combination of cited references does not teach determining if a first write data stored in a register is different from a second write data of a pending write request stored in the register, as recited in the claim. In particular, Norman does not teach determining if first write data stored in a register is different from second write data of a pending write request stored in the register because Norman does not teach using data of a pending write request. Magro also fails to teach determining if a first write data stored in a register is different from a second write data of a pending write request stored in the register because Magro does not compare write data.

1. Norman does not teach comparing first write data in a register with second write data of a pending write request stored in the register.

Norman does not teach determining if first write data stored in a register is different from second write data of a pending write request stored in the register because Norman does not teach using data of a previous, pending write request.

Norman merely describes a controller which fetches and compares a byte of data ("preread" data) from a flash memory array and a corresponding byte of data from buffer memory. Norman, col. 9, line 66, through col. 10, line 1. If the comparison result indicates that two sectors of data from the flash memory array and the buffer memory are the same, then there is no need to write the new data to the flash memory array. Norman, col. 10, lines 37-42. On the contrary, if the comparison result indicates that the two sectors of data from the flash memory array and the buffer memory are different, then the

controller will write the new set of data from the buffer memory to a new sector of the flash memory array. Norman, col. 10, lines 30-34.

Although Norman may describe comparing two sectors of write data, the write data from the buffer memory is not compared with write data from a pending write request. Rather, the write data from the buffer memory is specifically compared with data fetched from the flash memory array. Since the data in the flash memory array is previously stored data (Norman, col. 1, lines 12-21), the data in the flash memory array does not correspond to a pending write request because the controller is not waiting to write the previously stored data to the flash memory array. Therefore, even though the previously stored data may be read to the flash interface, the write data from the buffer memory is not compared with data that is part of a pending write request because the data in the flash memory array does not correspond to a pending write request.

Also, it should be noted that Norman does not teach storing write data from first and second write requests, as recited in the claim, in a single register or other temporary storage location. Rather, Norman specifically teaches that the current write data is stored in the buffer memory, while the preread data is read via the flash interface. Norman, Fig. 3. Although the buffered data and the preread data are input to the comparator (as inputs "A" and "B," respectively), Norman does not describe storing the buffered data and the preread data on a single memory device. Therefore, the description of the buffer memory and the separate flash interface in Norman is contrary to the requirement that the current write data and the previous write data of a pending write request are stored on the same memory device.

2. Magro does not teach comparing first write data with second write data of a pending write request in the register.

Although the Office Action does not rely on Magro as teaching the operation of comparing first and second write data, for the sake of providing a complete response Applicant nevertheless includes some discussion of why Magro does not teach limitations, as recited in the claim. As explained in Applicant's previous responses, Magro does not teach comparing first and second write data in a register to determine if the first and second write data are different. Magro merely describes determining which

bits are valid, but Magro does not determine if the content of the first and second write data are different.

Magro is directed to a system with a write buffer to provide random access snooping capability. Magro, abstract. More specifically, Magro describes a random access memory (RAM) 80 with a content addressable memory (CAM) address store 68 and a RAM data store 70. Magro, Fig. 2. A producer provides the address store with an input write address and provides the data store with input write data. The CAM compares the input write address to the addresses in the address store to determine if the input write address is "related" to an address present in the address store. If the input address is related to an address in the address store, then the input write data is stored in the rank of the data store associated with the related address in the address store. Magro, col. 2, lines 20-37.

Magro describes two ways to store the input write data in the data store. For input write data that does not overlap with the data already stored in the rank of the data store, a write merging operation merges the input write data with the existing write data in the data store. Magro, col. 2, lines 37-40. An example of write merging is explained in relation to Fig. 3E, in which the input write data '---52cc' is merged with the existing write data 'a369----' to produce write data 'a36952cc' in the data store. Magro, col. 10, lines 19-23. For input write data that overlaps with the data already stored in the rank of the data store, a write collapse operation overwrites the corresponding write data in the data store using the input write data. Magro, col. 2, lines 40-43; col. 12, lines 34-37. An example of write collapsing is explained in relation to Fig. 4E, in which the input write data '---52cc' partially overwrites the existing write data 'a36941ff' to produce write data 'a36952cc' in the data store (i.e., the '41ff" portion of the existing write data is overwritten by the input write data '52cc'). Magro, col. 12, lines 16-25.

Although Magro describes write merging and write collapsing to place the input write data in the data store, Magro does not describe comparing the input write data with the existing write data already in the data store. Rather, Magro merely describes using valid bits to indicate whether the existing write data is valid. Magro, col. 12, lines 20-37. In the examples referred to above, the invalid write data designated by dashes '----' would not have the corresponding valid bits set, while the valid write data would have the

corresponding valid bits set. However, the valid bits are not used for any type of comparison between the input write data and the existing write data already in the data store. Thus, even if Magro were to describe ascertaining whether an input write address is stored in the address store, Magro nevertheless does not describe comparing the input write data with the existing write data already in the data store.

Moreover, the write merging and write collapsing described in Magro does not inherently teach comparing the input write data with the existing write data already in the data store. As indicated above, Magro merely indicates using valid bits to designate whether or not the data store includes existing data. While Magro describes two types of writing operations, there is no difference between these two types of writing operations which would support the assertion of an inherent comparison. Regardless of whether the writing operation is considered a write merging operation or a write collapsing operation, the described functionality merely writes the new data to the corresponding locations within the memory store, without any type of comparison.

Therefore, the combination of Norman and Magro does not teach all of the limitations of the claim because neither Norman nor Magro teaches comparing first write data with second write data of a pending write request stored in the register, as recited in the claim. Accordingly, Applicant respectfully asserts claim 1 is patentable over the combination of Norman and Magro because the combination of Norman and Magro does not teach all of the limitations of the claim.

Independent Claim 17

Applicant respectfully asserts independent claim 17 is patentable over the combination of Norman and Magro at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 17 recites "ascertaining whether said first address information is equal to second address information for a pending write request stored in said writing queue, wherein said pending write request comprises said second address information and corresponding second write data" and "if yes, determining if said first write data stored in said register is

different from said second write data of said pending write request stored in said register" (emphasis added).

Here, although the language of claim 17 differs from the language of claim 1, and the scope of claim 17 should be interpreted independently of claim 1, Applicant respectfully asserts that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 17. Accordingly, Applicant respectfully asserts claim 17 is patentable over the combination of Norman and Magro because the combination of Norman and Magro does not teach comparing first write data with second write data of an earlier write request in the register, as recited in the claim.

Dependent Claims

Claims 2-15 and 18-25 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 17. Applicant respectfully asserts claims 2-15 and 18-25 are allowable based on allowable base claims. Additionally, each of claims 2-15 and 18-25 may be allowable for further reasons.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the proposed amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

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Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111